UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/492,789	01/28/2000	Takakazu Yano	01165.0770	1372

22852 7590 07/02/2003

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
1300 I STREET, NW
WASHINGTON, DC 20005

EXAMINER
JORGENSEN, LELAND R

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 07/02/2003

16

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/492,789	YANO ET AL.	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 16 and 18* is/are pending in the application.

4a) Of the above claim(s) *17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 16 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. In view of applicant's amendment dated 29 May 2003, the objection to claim 13 is withdrawn.

Claim Rejections - 35 USC § 112

2. In view of applicant's argument made in the amendment dated 29 May 2003, the rejection of claims 5 and 6 under 35 U.S.C. 112, first paragraph, is withdrawn.

3. In view of applicant's amendment and argument made in the amendment dated 29 May 2003, the rejection of claims 4 – 6 under 35 U.S.C. 112, second paragraph, is withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Woodside et al., USPN 4,390,874.

Claim 1 (twice amended)

Woodside teaches a power supply circuit. The power supply circuit includes a voltage regulation circuit [voltage regulator 18] and a temperature compensation circuit [temperature compensator 24] for compensating a temperature characteristic of the liquid crystal display

device [LCD display 20] by changing the voltages provided to the common lines of the display. Woodside, col. 1, lines 18 – 32; col. 2, lines 30 – 54; and figure 1. Woodside teaches that the voltage regulator provides scan drive voltage to a scan driver [common control 16] and data driver voltage to a data driver [segment control 22].

Claim 18

Woodside teaches a power supply circuit with a voltage regulation circuit [voltage regulator 18] and a temperature compensation circuit [temperature compensator 24]. Woodside, col. 1, lines 18 – 32; col. 2, lines 30 – 54; and figure 1. Fujii teaches a voltage regulation function and a power supply function for the liquid crystal display. Fujii, col. 4, lines 1 – 3; col. 5, lines 15 – 24, 29 – 36; and figures 1 and 2. It is inherent that the data driver power circuit described by Woodside and Sakamoto would perform these functions at the same time.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2 – 6 and 9 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woodside et al., in view of Fujii et al., USPN 5,663,743, and in view of Sakamoto et al., USPN 3,956,661.

Claim 2 (amended)

Woodside shows input power supply. Woodside, figure 1. The temperature compensator is connected to the voltage regulator and the voltage regulator is connected to the common control and segment control of the liquid crystal display.

Woodside does not teach the amplifying element as taught in claim 2.

Fujii teaches the amplifying element. The specification gives an example of an amplifying device being a bipolar transistor with the collector being the input terminal, the base being the control terminal, and the emitter being the output terminal. Fujii shows a transistor Tr with a collector, base, and emitter. Fujii, figure 1; and col. 6, lines 4 - 12. Fujii shows a variable resister R1 that has a portion of the resistance between the input power supply and the control terminal of the amplifying element. Fujii, figure 1; and col. 6, lines 4 – 11. Fujii teaches that the data driver power circuit includes input power supply V_{CC} serving as a universal power supply. Fujii, figure 1; col. 5, lines 29 – 36; and col. 6, lines 4 – 8.

Fujii teaches a power supply circuit [voltage supply circuit 24] including a scan power supply circuit to supply scan drive voltage [V1, V3, and V5] to a scan driver [level scanning line driver 23] for scanning a liquid crystal display. Fujii, col. 4, lines 1 – 3; col. 5, lines 22 – 24, 29 – 36; and figures 1 and 2. A data power supply circuit supplies data drive voltage [V2 and V4] to a data driver [level data line driver 22] for sending display data to a liquid crystal display. Fujii, col. 4, lines 1 – 3; col. 5, lines 15 – 17, 29 – 36; and figures 1 and 2.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the amplifying element as taught by Fujii with the power supply circuit of Woodside. Fujii invites such combination by teaching,

> In general, a liquid crystal display needs data line drivers and scanning line drivers for providing the driving waveforms as alternating waveforms, and a voltage supply circuit for these data line drivers and scanning line drivers.

Fujii, col. 1, lines 42 – 45. Fujii teaches the first object of its invention.

> Therefore, the first object of this invention is to provide a new dynamic scattering matrix LCD which is low in the expenditure of electric power without deteriorating the contrast, even when it is used for a high-speed response STN liquid crystal display.

Fujii, col. 2, lines 26 – 30. Fujii teaches the second object of its invention.

> So, the present invention can reduce the expenditure of electric power to 1/3 lower than that of a conventional LCD.
>
> Further, the second object of this invention is to provide a new dynamic scattering matrix LCD which is a high-speed response STN LCD having the capability of displaying moving image data like a mouse cursor moving quickly in a display window.

Fujii, col. 3, lines 43 – 49. Fujii concludes,

> It will be understood from this formula that the expenditure of electric power is 1/3 lower than that of the conventional LCD.

Fujii, col. 7, lines 14 – 16. Fujii adds,

> As mentioned above, in the described embodiments, the LCD expends only a small electric power.

Fujii, col. 7, lines 34 – 35.

Neither Woodside nor Fujii specifically teach that the temperature compensation circuit is connected to the control terminal of the amplifying element.

Sakamoto teaches a voltage regulation circuit and temperature compensation circuit.. Sakamoto, figure 1; col. 2, lines 22 – 33. The temperature compensation circuit is connected to the control terminal of an amplifying element, a transistor 1 with a collector, base, and emitter. Sakamoto, figure 2; col. 2, lines 22 – 33.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the voltage regulation and temperature compensation circuit of Sakamoto with the data drive power circuit of Fujii to create a temperature compensation data drive power circuit. Sakamoto invite such combination by teaching,

> The present invention relates to an improved D.C. power source for stabilizing an output voltage and/or current especially in integrated circuits (IC) and also for compensating for deviation or fluctuation in the current amplification factor h_{FE} or β of a transistor due to variation in the ambient temperature.
>
> Heretofore, in a transistor circuit for supplying constant output voltage, a power supply voltage was divided by a pair of bias resistors including an emitter resistor in a transistor circuit built in an integrated circuit block, and the divided voltage was supplied to a transistor or transistors also built in the integrated circuit blocks. However, in a prior D.C. power source the compensation for preventing the change of the output voltage due to temperature change was not enough because the values of the resistances in the IC blocks were considerably varied by discrepancies among resistors as well as temperature variations, and it was very difficult to construct a transistor circuit in which an absolute value of the current flowing through a load was maintained constant.

Sakamoto et al., col. 1, lines 5 – 10. Sakamoto adds,

> A main purpose of the present invention is, therefore, to provide a D.C. power source having a temperature compensation circuit in which variation in the voltage drop between the base and emitter of a transistor due to variation in the ambient temperature is compensated.
>
> Another purpose of the present invention is to provide a D.C. power source having a temperature compensation circuit in which variation or deviation of the current amplification factor h_{FE} or β due to variation in the ambient temperature is compensated.
>
> A still further purpose of the present invention is to provide a D.C. power source having a temperature compensation circuit in which the effect of variation in the ambient temperature on the output voltage and/or current compensated.

Sakamoto, col. 1, lines 29 – 45.

Claim 3 (amended)

Sakamoto teaches that the voltage regulation circuit and the temperature compensation circuit comprise a diode group having a plurality of series connected diodes connected between the control terminal of the amplifying element and ground. Sakamoto, figure 1; col. 2, lines 22 – 33.

Claim 4 (amended)

Sakamoto teaches that the series-connected diodes with a first diode having a cathode terminal connected to the control terminal of the amplifying element and a second diode with an anode terminal connected to the ground respectively. Sakamoto, figure 1; col. 2, lines 22 – 33.

Claim 5 (amended)

Sakamoto teaches a circuit where the sum of the voltage drop of each diode, the voltage V_{B1} at the junction point (a), is equal to the data driver voltage V_{E1}. Sakamoto, col. 4, lines 2 – 6.

Claim 6 (amended)

It would have been obvious to one of ordinary skill in the art at the time of the invention to use seven diodes in the diode group. Sakamoto invites one to vary the number of diode. After defining *m* as the number of diode between the control terminal and ground, Sakamoto states,

> As described above, whenever the dividing ration of the D.C. power supply voltage V_{CC} is desired, the first and second resisters R1 and R2 and values of *m* and *n* are in turn determined. Thus the effect of the change of the voltage drop between the base and emitter V_{BE} of the transistor 1 due to temperature change is completely avoided by inserting a predetermined number of diodes 6.

Sakamoto, col. 3, lines 17 – 24. For one of ordinary skill in the art at the time of the invention, it is an obvious design choice, as motivated by the above teachings of Sakamoto, to choose a certain number of diodes to set an appropriate voltage drop.

Claim 9 (amended)

Sakamoto teaches that the amplifying elements are transistors. Sakamoto, figure 2, col. 2, lines 22 – 33. Although Sakamoto does not specifically state in the specifications that the transistors are bipolar, bipolar transistors would be inherent because the symbol of the transistor used in Sakamoto's figures are those typically used for bipolar transistors.

Claim 10 (amended)

It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a range. Sakamoto invites one to consider different resistances. Sakamoto, col. 3, lines 17 – 24. Sakamoto offers formulas to find such resistances. Sakamoto, col. 2, line 21 – col. 3, line 32. For one of ordinary skill in the art at the time of the invention, it is an obvious design choice, as motivated by the above teachings of Sakamoto, to choose a certain resistance to produce an appropriate current.

Claim 11 (amended)

It would have been obvious to one of ordinary skill in the art at the time of the invention to use silicon diodes for the diodes of the diode group. Silicon diodes are readily available and well know in the art, as admitted in applicant's specification, page 2, lines 11 – 12.

8. Claims 7, 8, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable either over 1) Woodside in view of Nishioka et al., USPN 6,121,943, or over 2) Woodside, Sakamoto et al., and Fujii et al., as applied to claim 2 above, and further in view of Nishioka et al.

Claim 7 (amended)

Woodside does not teach a divider circuit or a variable resister.

Nishioka teaches divider circuit. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5. Nishioka teaches a variable resister 81b having a resistance variation terminal connected to the control terminal of the amplifying element. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the constant current control circuit of Nishioka to the display voltage supply circuit of Woodside to create a scan driver power circuit. Nishioka points out that "It is an object of the present invention to solve the problems associated with the generation of heat and the rush current during the application of the scan signal while reducing the charging and discharging time." Nishioka, col. 1, lines 54 – 57. Nishioka teaches the advantage of its power circuit for scan driver. "Thus, the constant current control circuit 81 performs control to provide a constant current in response to the control signal at a high level input from the input terminal S1. Nishioka, col. 6, lines 2 – 5.

Claim 8 (amended)

Nishoika teaches a resister 81c having a terminal connected to the input power supply. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5. Nishioka teaches a Zener diode 81d

having a cathode connected to the resister and an anode to ground. Nishioka, figures 4 and 6 and col. 6, lines 19 – 21.

Claim 14

Nishioka teaches the use of bipolar transistors in the scan driver and the data driver. Nishioka, col. 8, lines 44 – 48.

Claim 15

Nishioka teaches the use of field effect transistors (FET). Nishioka, col. 5, line 59 – col. 6, line 5.

9. Claim 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woodside, Sakamoto et al., and Fujii et al., as applied to claim 2 above, and further in view of The Electrical Engineering Handbook.

Claims 12 and 16

Sakamoto teaches a transistor. Sakamoto, figure 2, col. 2, lines 22 – 33. Nishioka teaches the use of field effect transistors (FET). Nishioka, col. 5, line 59 – col. 6, line 5. Fujii teaches MOS transistors. Fujii, figure 1; and col. 6, lines 12 – 14.

Sakamoto does not teach that the transistors are MOS transistors and Fujii uses the MOS transistors in a slightly different way in the circuit.

The Electrical Engineering Handbook teaches the use of MOS transistors. Handbook, p. 567 – 580.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use MOS transistors for transistors in the data driver power circuit of Sakamoto. The

Handbook teaches that MOS transistors allow easy fabrication using lithographic processes, resulting in integrated circuits (ICs), with very small devices, very large device counts, and very high reliability at low cost. MOS transistors also allow manufacture of complex systems without expensive packaging or cooling requirements. Handbook, p. 568.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woodside, Sakamoto et al., and Fujii et al., as applied to claim 2 above, and further in view of Ishizaki et al., USPN 5,473,289.

Claim 13

Sakamoto does not teach the use of operational amplifiers. Fujii teaches operational amplifiers but in a slightly different way than described in claim 13. Fujii, figure 1 and col. 6, lines 31 – 34.

Ishizaki, however, teaches the use of a temperature control circuit 101 having a operational amplifier with the control terminal connected to a plurality of diodes to ground and a resister to the voltage source. Ishizaki, figure 6(b), col. 7, lines 49 – 57.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the temperature control circuit of Ishizaki with the data driver power circuit of Woodside, Fujii, and Sakamoto. Ishizaki teaches that such a circuit "generates a voltage which is proportion to the detected voltage." Ishizaki, col. 7, lines 29 – 30. See also Ishizaki, col. 8, lines 2 – 7; and figure 3. One would be motivated to use the Ishizaki circuit because operational amplifiers are readily available and the Ishizaki circuit has a linear output.

Double Patenting

11. Applicant is advised that should claim 12 be found allowable, claim 16 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Response to Arguments

12. Applicant's arguments with respect to claims 1 – 16 and 18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Itoh et al., USPN 4,687,956; Klosterboer, USPN 4,807,972; and Matsuo et al., USPN 4,319,237 each teach a LCD driver with temperature control.

Walukas et al., USPN 6,107,985, teaches a backlight with temperature control.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

lrj

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600